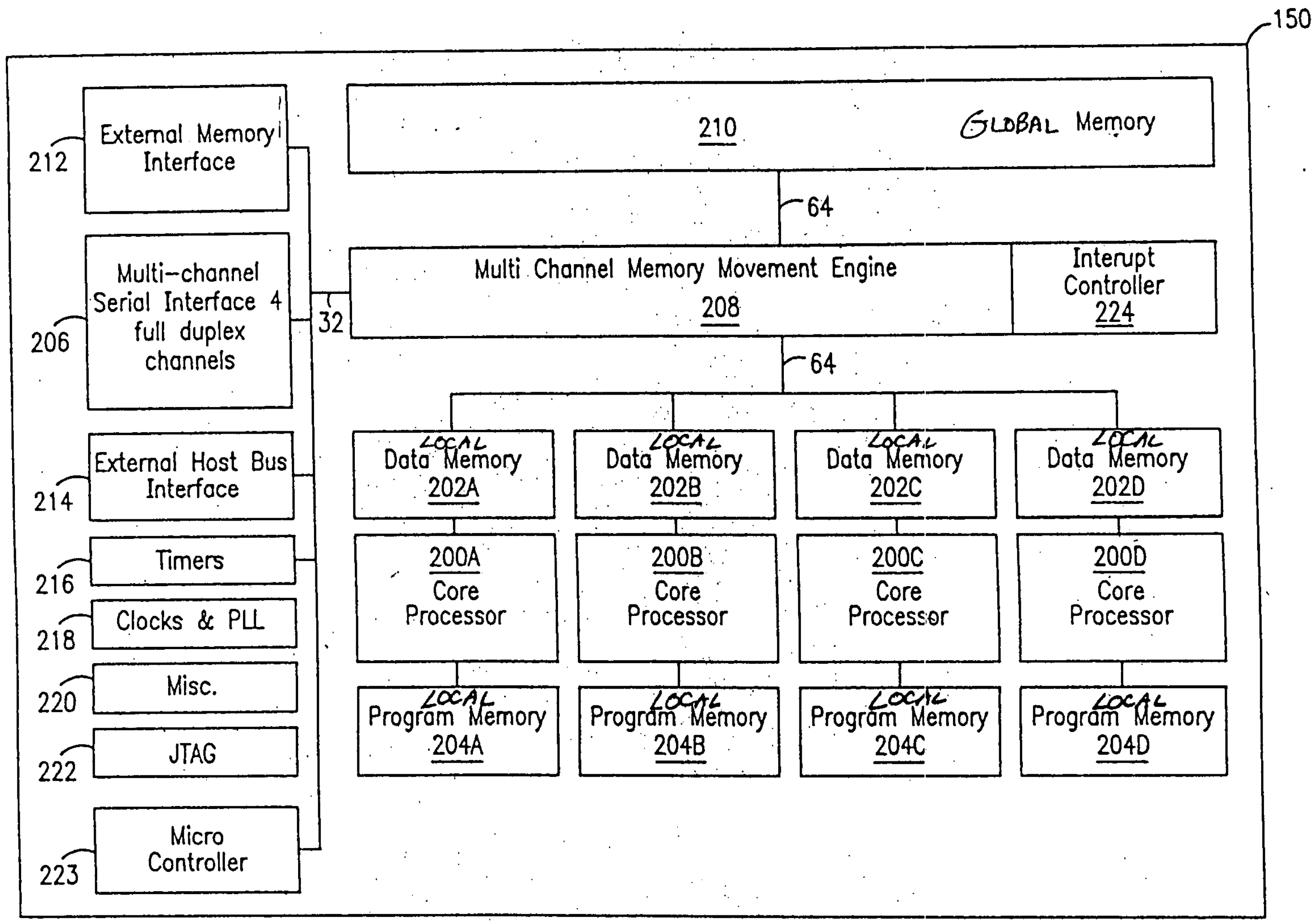
150
External Memory Interface
212
Multi-channel Serial Interface 4 full duplex channels
206
External Host Bus Interface
214
Timers
216
Clocks & PLL
218
Misc.
220
JTAG
222
Micro Controller
223
32
210
GLOBAL Memory
64
Multi Channel Memory Movement Engine
208
Interupt Controller
224
64
LOCAL Data Memory 202A
LOCAL Data Memory 202B
LOCAL Data Memory 202C
LOCAL Data Memory 202D
200A Core Processor
200B Core Processor
200C Core Processor
200D Core Processor
LOCAL Program Memory 204A
LOCAL Program Memory 204B
LOCAL Program Memory 204C
LOCAL Program Memory 204D

FIG. 1

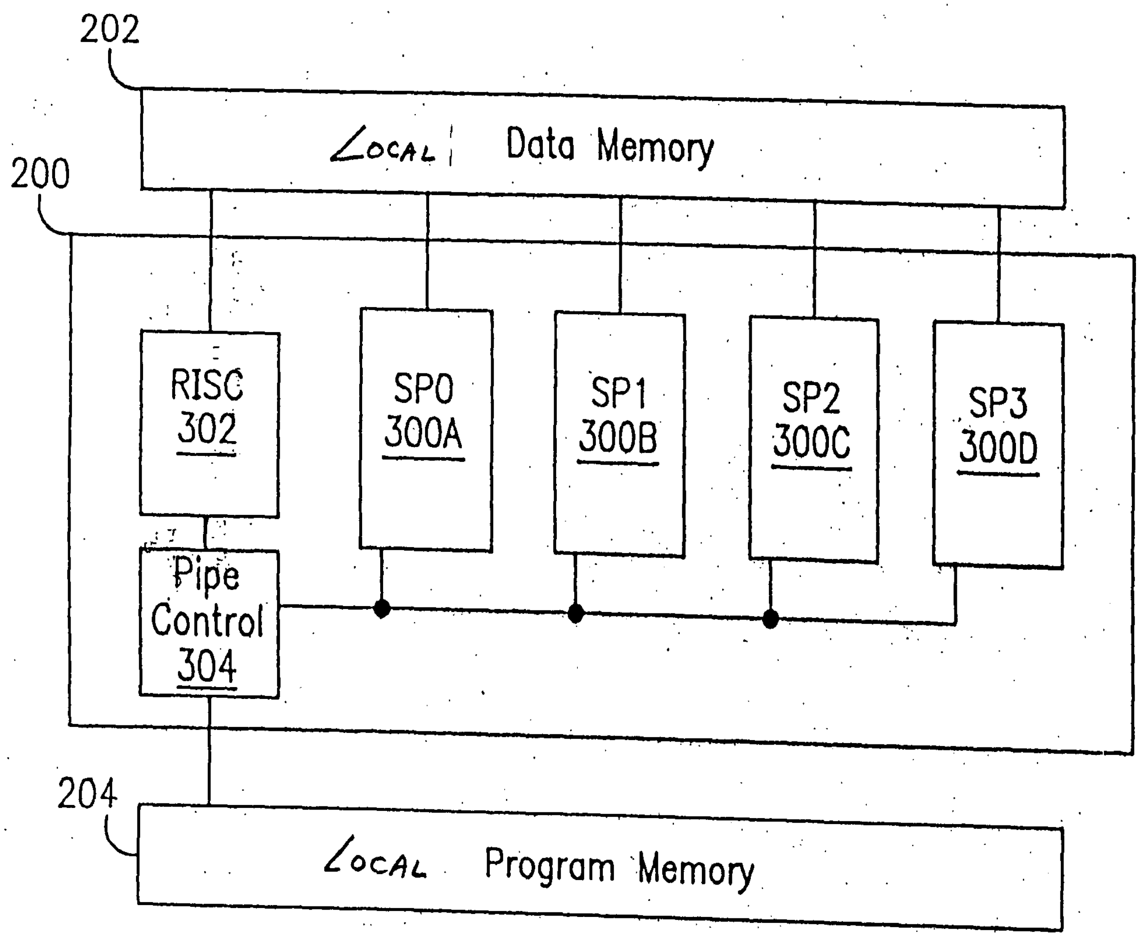
202
LOCAL Data Memory
200
RISC
302
SP0
300A
SP1
300B
SP2
300C
SP3
300D
Pipe
Control
304
204
LOCAL Program Memory

FIG. 2

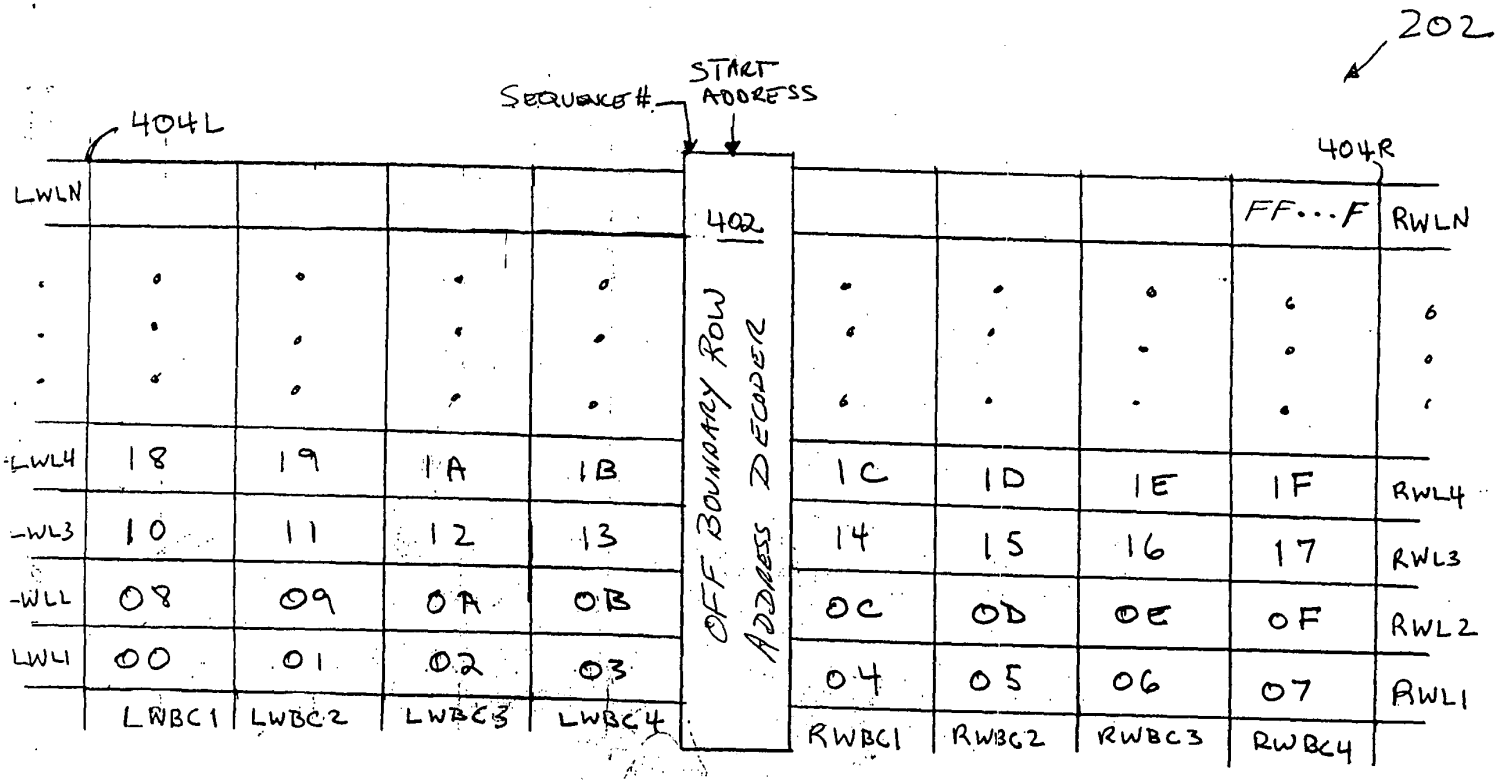
202
404L
SEQUENCE #
START ADDRESS
404R
402
OFF BOUNDARY ROW ADDRESS DECODER
LWLN
-LWL4
-WL3
-WLL
LWL1
RWLN
RWL4
RWL3
RWL2
RWL1
FF...F
18 19 1A 1B 1C 1D 1E 1F
10 11 12 13 14 15 16 17
08 09 0A 0B 0C 0D 0E 0F
00 01 02 03 04 05 06 07
LWBC1 LWBC2 LWBC3 LWBC4
RWBC1 RWBC2 RWBC3 RWBC4

FIG. 3A

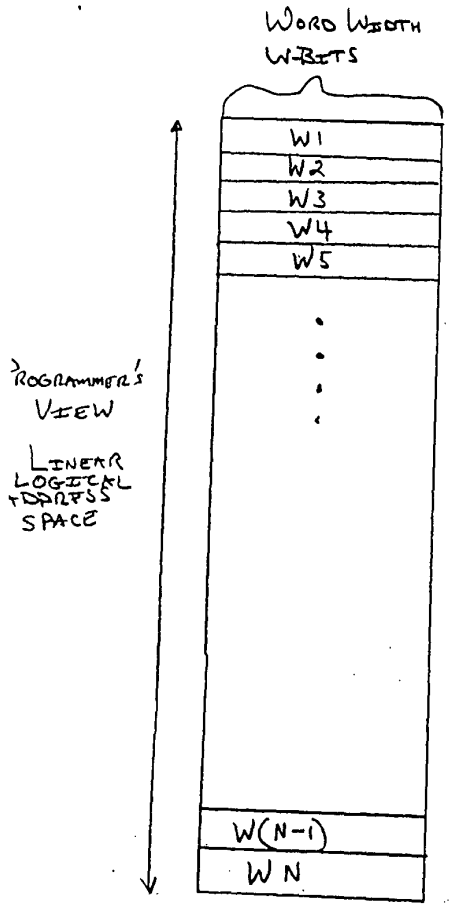

FIG. 3B

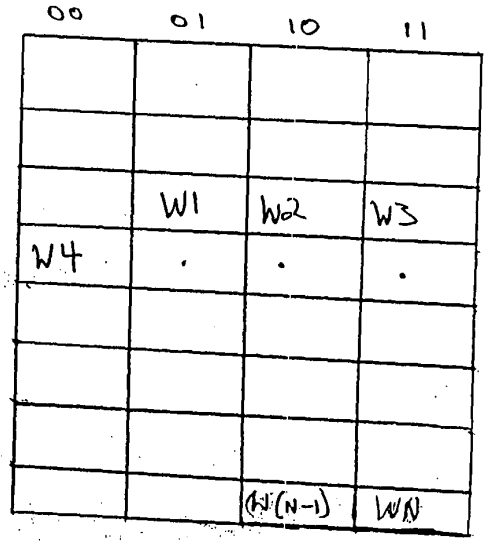

FIG. 3C

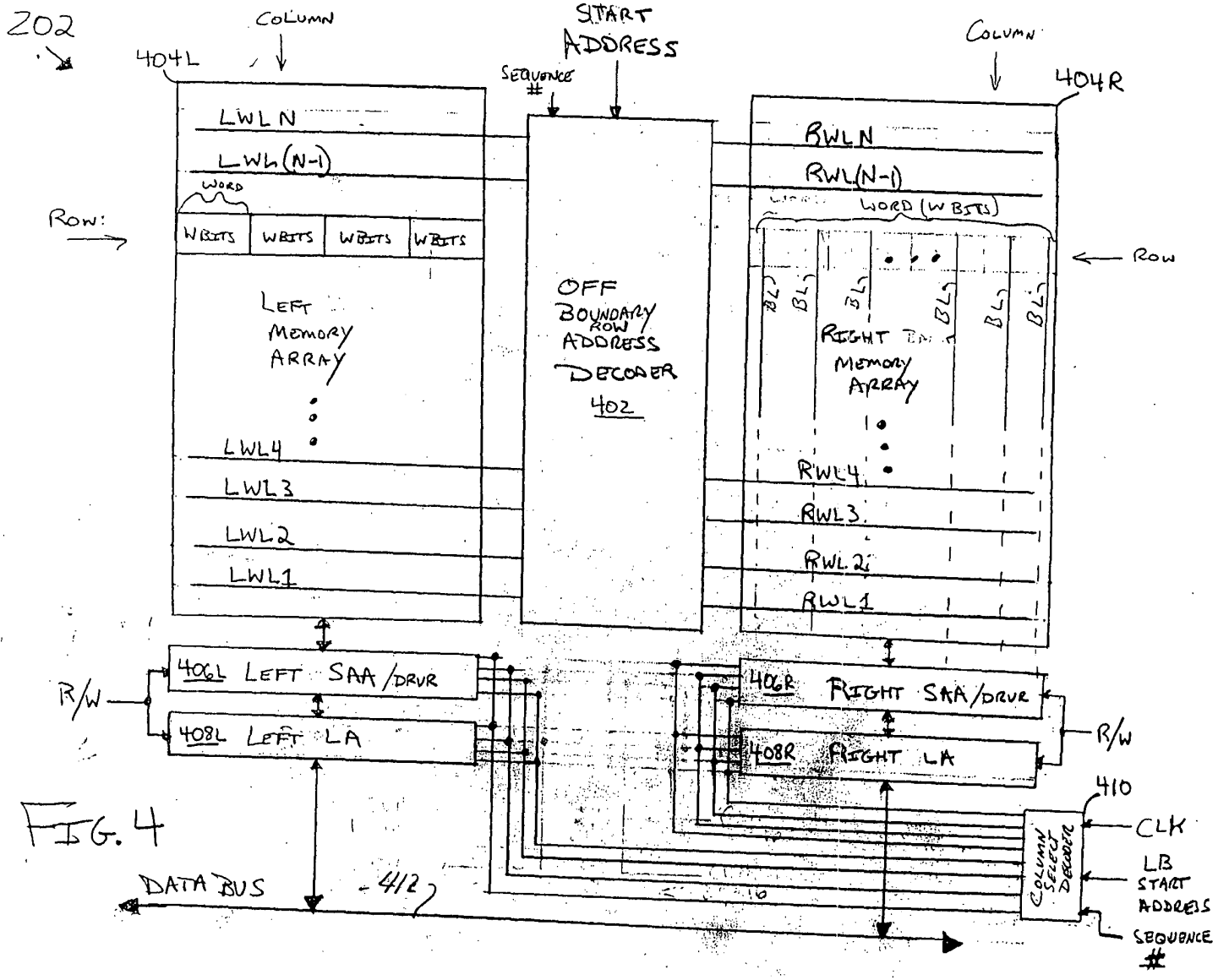
202
COLUMN
404L
START ADDRESS
SEQUENCE #
COLUMN
404R
LWLN
LWL(N-1)
WORD
ROW
WBITS
WBITS
WBITS
WBITS
LEFT MEMORY ARRAY
OFF BOUNDARY ROW ADDRESS DECODER 402
RWLN
RWL(N-1)
WORD (W BITS)
ROW
BL
RIGHT MEMORY ARRAY
LWL4
LWL3
LWL2
LWL1
RWL4
RWL3
RWL2
RWL1
R/W
406L LEFT SAA/DRVR
408L LEFT LA
406R RIGHT SAA/DRVR
408R RIGHT LA
R/W
410
CLK
LB START ADDRESS
SEQUENCE #
COLUMN SELECT DECODE
DATA BUS
412

FIG. 4

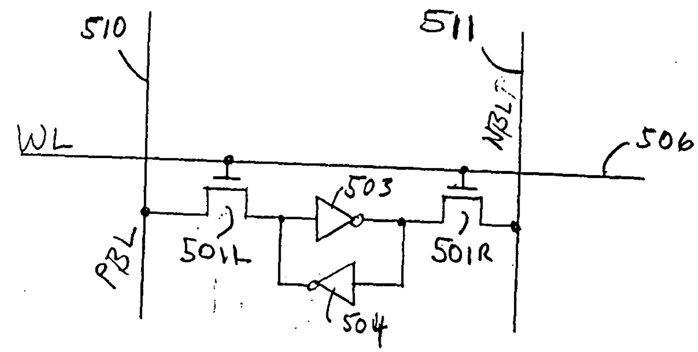

FIG. 5A

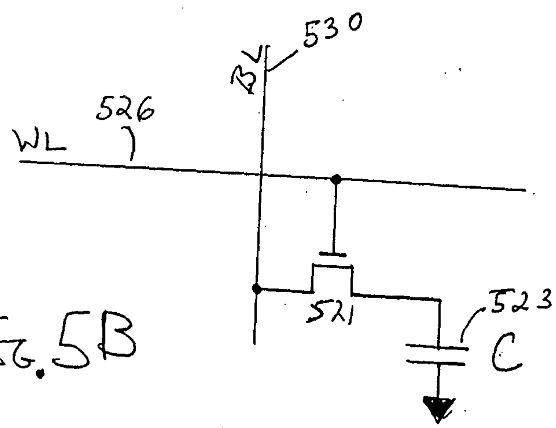

FIG. 5B

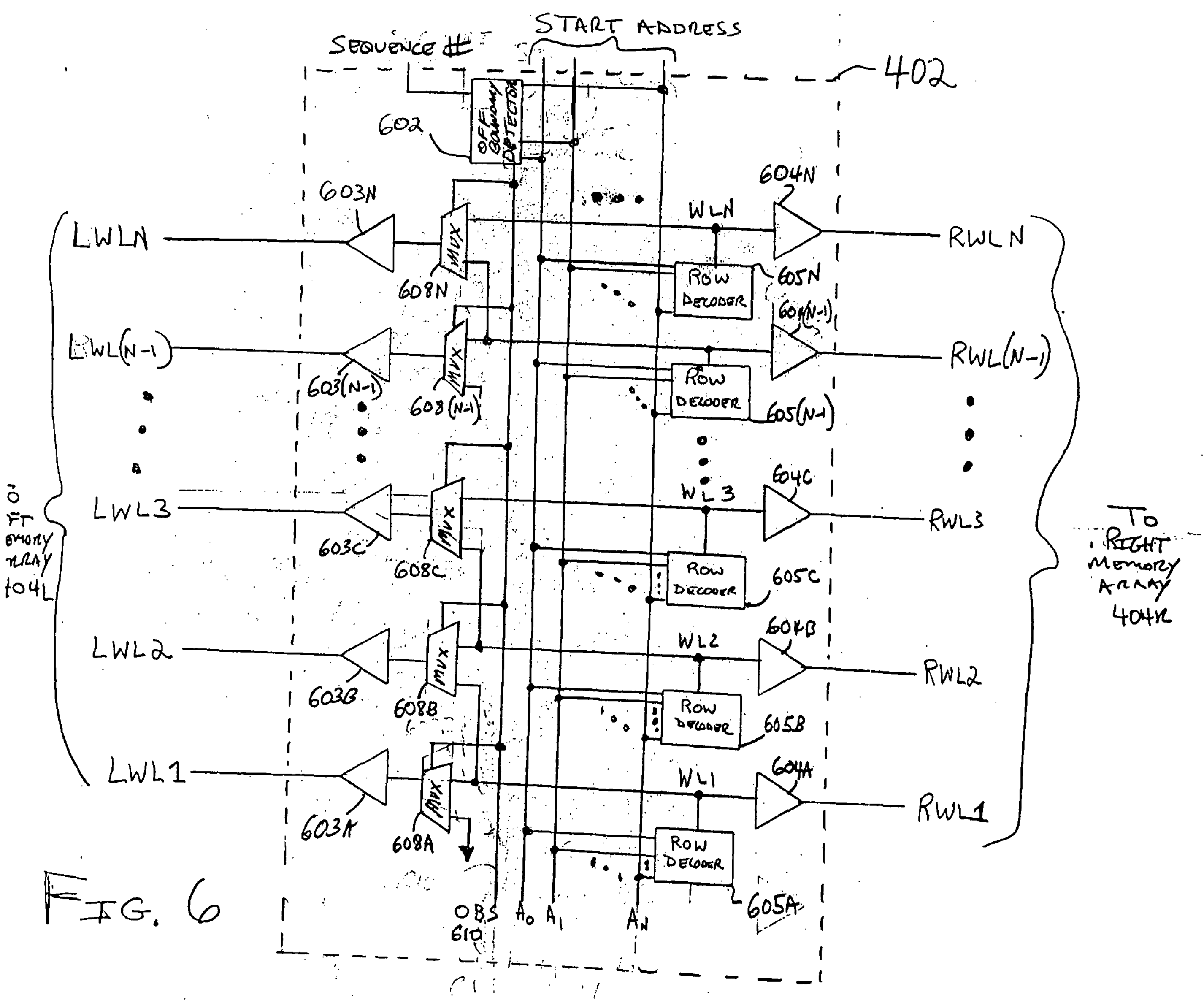

FIG. 6